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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,133	09/30/2003	David Arthur James Webb JR.	200301788-2	5703

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HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER

LOHN, JOSHUA A

ART UNIT	PAPER NUMBER
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2114

DATE MAILED: 12/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/675,133	Applicant(s) WEBB ET AL.	
	Examiner Joshua A. Lohn	Art Unit 2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 3-5, 10-12, 15 and 17-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 3, 4, 10, 11 and 15 is/are rejected.
- 7) ☒ Claim(s) 5, 12 and 17-21 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>9/30/03</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION***Double Patenting***

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 3, 4, 10, 11, and 15 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1, 3, and 5 of U.S. Patent No. 6,662,319. Although the conflicting claims are not identical, they are not patentably distinct from each other.

Claim 3 of the instant application is not patentability distinct because claim 1 of the patent discloses the limitations of “a computer system, comprising: a plurality of processors coupled together between which messages can be routed; an I/O controller coupled to one or more of said processors; at least one I/O device coupled to an I/O controller; and wherein each processor is capable of detecting an error in a message sent from another processor in the system and reformatting the message to indicate to other of said processors that the message contains a

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transmission error”. Claim 1 of the patent does not explicitly disclose “wherein each of said messages between said processors comprises a header ticks and data tick, the data tick comprising error check bits and wherein upon detecting an error has occurred in the message, the processor alters the data tick error check bits in a predetermined manner to indicate to other of said processors that the message contains an error”, however claim 1 does disclose the use of multiple ticks that can include the data tick and error check bits mentioned above. Claim 1 does not recite the use of a header tick, but it is inherent in the operation message routing that some form of header tick must be used in the determination of message destination. Claim 1 of the patent further discloses the altering of the data tick by replacing the bits with a predetermined sequence upon detection of an error, this would include the error check bits of each data tick as required by claim 3 of the instant application. As shown above, claim 1 of the patent obviously discloses a form of the limitations of claim 3 of the instant application, thus showing that claim 3 is not patentability distinct.

Claim 4 of the instant application is not patentability distinct because claim 1 of the patent discloses the limitations of “a computer system, comprising: a plurality of processors coupled together between which messages can be routed; an I/O controller coupled to one or more of said processors; at least one I/O device coupled to an I/O controller; and wherein each processor is capable of detecting an error in a message sent from another processor in the system and reformatting the message to indicate to other of said processors that the message contains a transmission error”. Claim 1 of the patent does not explicitly disclose “wherein each of said messages between said processors comprises a header ticks and data tick, each tick comprising

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multiple bits of information, and wherein upon detecting an error has occurred in a data tick, the processor replaces the bits of information in the data tick with a predetermined bit pattern”, however claim 1 does disclose the use of multiple ticks that can include the data tick mentioned above. Claim 1 does not recite the use of a header tick, but it is inherent in the operation message routing that some form of header tick must be used in the determination of message destination. Claim 1 of the patent further discloses that upon the detection of an error, the bits of the tick are replaced with a predetermined bit pattern. This replacement of the bits of a tick in claim 1 of the patent would obviously include all types of ticks, including the data ticks of claim 4 of the instant application. Thus it is shown that claim 1 of the patent obviously discloses a form of the limitations of claim 4 of the instant application, which is not patentability distinct.

Claim 10 of the instant application is not patentability distinct because claim 3 of the patent discloses the limitations of “a processor, comprising: a memory controller that coordinates transactions to a memory device; and a router coupled to said memory controller and providing interfaces to one or more other processors; wherein said router is capable of detecting a transmission error in a message received from another processor and reformatting the message to indicate that the message contains a transmission error that has already been detected”. Claim 3 of the patent also discloses a data block comprising error check bits, and wherein upon detecting that a transmission error has occurred in the message, the router replaces all the bits of the data block with a predetermined bit pattern. This replacement is equivalent to altering the error check bits in a predetermined manner to indicate a transmission error, because the replacement of all the bits would include any error check bits. The only remaining difference is

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in claim 10 of the instant application, where the message comprises a data block, and in claim 3 of the patent, where the message comprises multiple sequential blocks of data. With regard to the additional blocks of data in claim 3 of the patent, which are not included in claim 10 of the instant application, the omission of these limitations in claim 10 of the instant application is an obvious expedient since the remaining limitations of claim 3 of the patent, referring to each block of data, perform the same function as the limitations in claim 10 of the instant application (*In re Karlson*, 136 USPQ 184 (CCPA 1963)).

Claim 11 of the instant application is not patentability distinct because claim 3 of the patent discloses the limitations of “a processor, comprising: a memory controller that coordinates transactions to a memory device; and a router coupled to said memory controller and providing interfaces to one or more other processors; wherein said router is capable of detecting a transmission error in a message received from another processor and reformatting the message to indicate that the message contains a transmission error that has already been detected”. Claim 3 of the patent also discloses upon detecting that a transmission error has occurred, the router replaces all the bits of the data block with a predetermined bit pattern. Claim 3 of the patent fails to disclose the message having a data block and a header block. However it is well known in the art that a header is often essential in determining the proper routing of a data block. It would have been obvious at the time of the invention to include a header block as one of the multiple blocks of claim 3 of the patent to provide this routing information.

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Claim 15 of the instant application is not patentability distinct because claim 5 of the patent discloses the limitations of “(a) receiving a message; (b) detecting an error in said message; (c) replacing the erroneous portion of said message with a predetermined bit pattern to indicate to other processors in said system that an error has occurred in said message and said error has already been detected; and (d) transmitting the message to another processor in said system”. With regard to the additional limitations in claim 5 of the patent consisting of the details on the replacement of the data portions, which are not included in claim 15 of the instant application, the omission of these limitations in claim 15 of the instant application is an obvious expedient since the remaining limitations of claim 5 of the patent perform the same function as the limitations in claim 15 of the instant application (*In re Karlson*, 136 USPQ 184 (CCPA 1963)).

Allowable Subject Matter

Claims 5, 12, and 17-21 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua A. Lohn whose telephone number is (571) 272-3661. The examiner can normally be reached on M-F 8-4.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAL



**SCOTT BADERMAN
PRIMARY EXAMINER**